ABSTRACT

A FinFET device and a method of lowering a gate capacitance and extrinsic resistance in a field effect transistor, wherein the method comprises forming an isolation layer comprising a BOX layer over a substrate, configuring source/drain regions above the isolation layer, forming a fin structure over the isolation layer, configuring a first gate electrode adjacent to the fin structure, disposing a gate insulator between the first gate electrode and the fin structure, positioning a second gate electrode transverse to the first gate electrode, and depositing a third gate electrode on the fin structure, the first gate electrode, and the second gate electrode, wherein the isolation layer is formed beneath the insulator, the first gate electrode, and the fin structure. The method further comprises sandwiching the second gate electrode with a dielectric material. The fin structure is formed by depositing an oxide layer over a silicon layer.